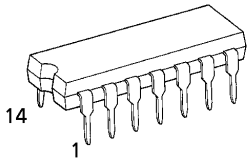
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC4071BP, TC4071BF, TC4071BFN

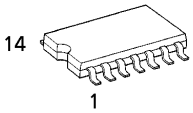
(Note) The JEDEC SOP (FN) is not available in Japan.

TC4071B QUAD 2 INPUT OR GATE

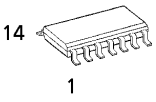
TC4071B is positive logic OR gates with two inputs respectively. As all the outputs of gates are equipped with the buffer circuits of inverters, the input / output propagation characteristic has been improved and the variation of propagation time caused by increase of load capacity is kept minimum.



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)



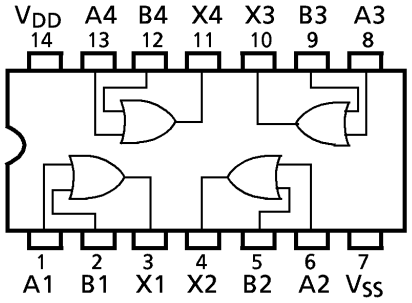
FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5\sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5\sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5\sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T_{opr}	−40~85	°C
Storage Temperature Range	T_{stg}	−65~150	°C

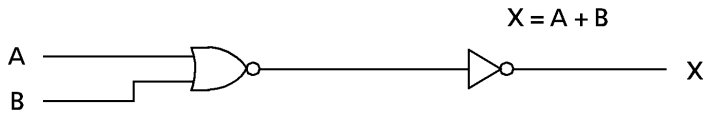
PIN ASSIGNMENT (TOP VIEW)

TC4071B



LOGIC DIAGRAM

1 / 4 TC4071B



980910EBA2

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	−40°C MIN.	−40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output High Current	I_{OH}	V_{OH} = 4.6V	5	−0.61	—	−0.51	−1.0	—	−0.42	—	mA
		V_{OH} = 2.5V	5	−2.50	—	−2.10	−4.0	—	−1.70	—	
		V_{OH} = 9.5V	10	−1.50	—	−1.30	−2.2	—	−1.10	—	
		V_{OH} = 13.5V	15	−4.00	—	−3.40	−9.0	—	−2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Output Low Current	I_{OL}	V_{OL} = 0.4V	5	0.61	—	0.51	1.5	—	0.42	—	
		V_{OL} = 0.5V	10	1.50	—	1.30	3.8	—	1.10	—	
		V_{OL} = 1.5V	15	4.00	—	3.40	15.0	—	2.80	—	
		$V_{IN} = V_{SS}$									
Input High Voltage	V_{IH}	V_{OUT} = 0.5V, 4.5V	5	3.5	—	3.5	2.75	—	3.5	—	V
		V_{OUT} = 1.0V, 9.0V	10	7.0	—	7.0	5.50	—	7.0	—	
		V_{OUT} = 1.5V, 13.5V	15	11.0	—	11.0	8.25	—	11.0	—	
		$\|I_{OUT}\| < 1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT} = 0.5V, 4.5V	5	—	1.5	—	2.25	1.5	—	1.5	
		V_{OUT} = 1.0V, 9.0V	10	—	3.0	—	4.50	3.0	—	3.0	
		V_{OUT} = 1.5V, 13.5V	15	—	4.0	—	6.75	4.0	—	4.0	
		$\|I_{OUT}\| < 1\mu A$									
Input Current "H"Level	I_{IH}	V_{IH} = 18V	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ *	5	—	0.25	—	0.001	0.25	—	7.5	
			10	—	0.50	—	0.001	0.50	—	15.0	
			15	—	1.00	—	0.002	1.00	—	30.0	

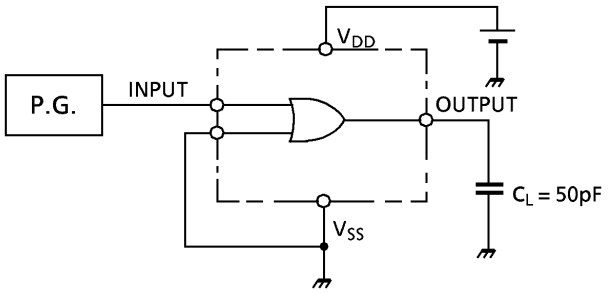
* All valid input combination

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, C_L = 50pF)

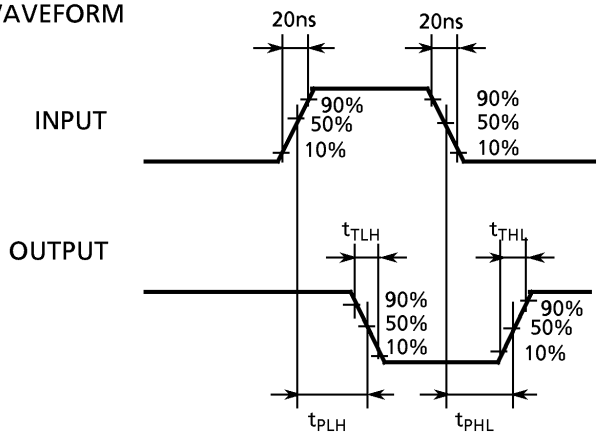
CHARACTERISTIC	SYMBOL	TEST CONDITION V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH}	5	—	70	200	ns
		10	—	35	100	
		15	—	30	80	
Output Transition Time	t_{THL}	5	—	70	200	
		10	—	35	100	
		15	—	30	80	
Propagation Delay Time	t_{pLH}	5	—	65	200	
		10	—	30	100	
		15	—	25	80	
Propagation Delay Time	t_{pHL}	5	—	65	200	
		10	—	30	100	
		15	—	25	80	
Input Capacitance	C_{IN}		—	5	7.5	pF

CIRCUIT A D WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

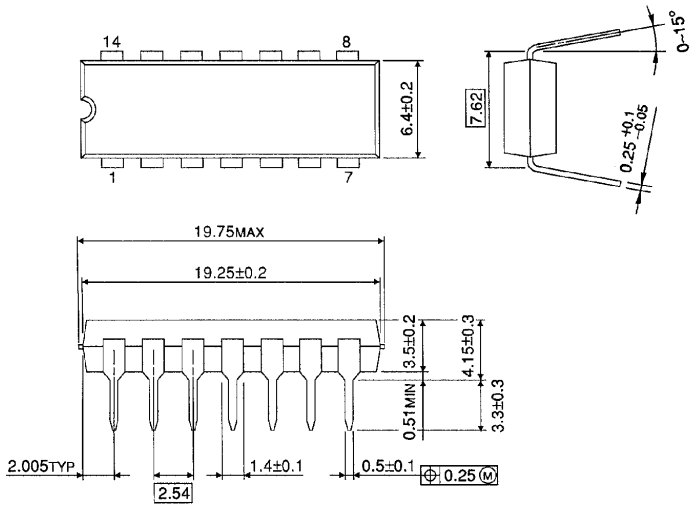
CIRCUIT



WAVEFORM

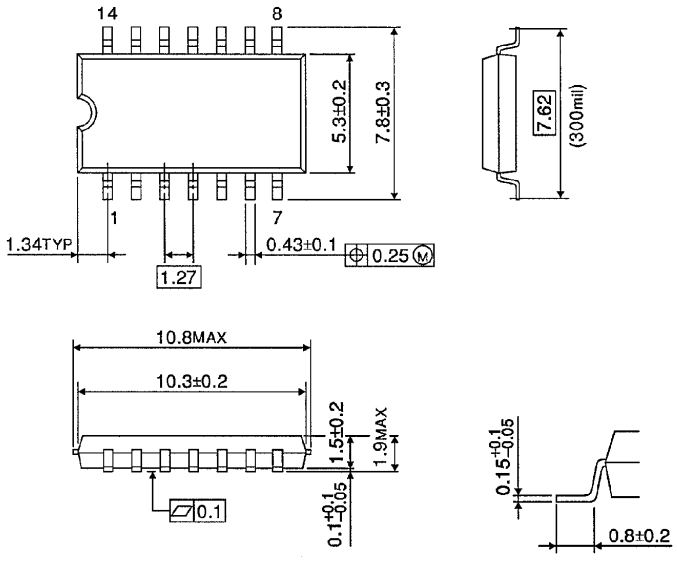


DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54) Unit in mm



Weight : 0.96g (Typ.)

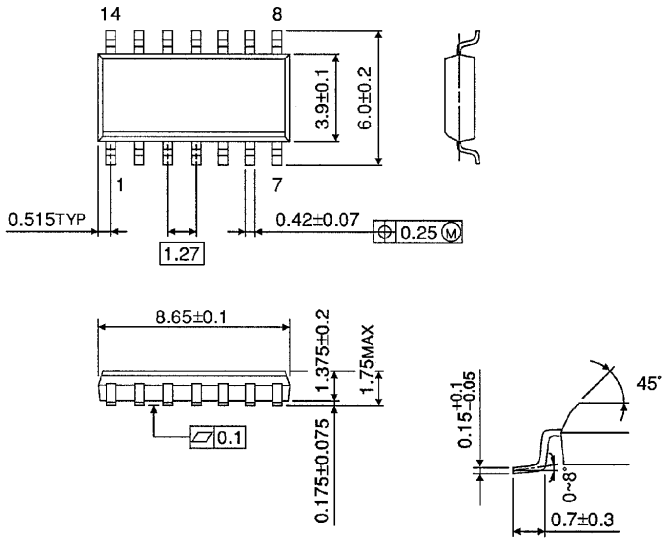
SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)