< Silicon RF Power Module >

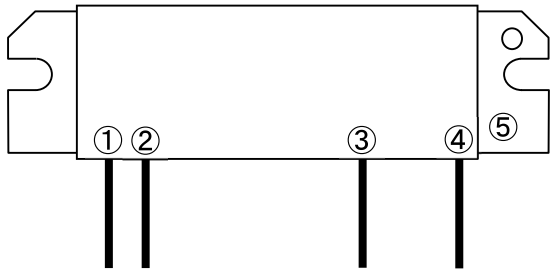
RA50H8994M1

RoHS Compliance, 896-944MHz 50W 12.5V, 2 Stage Amp. For Mobile Radio

DESCRIPTION

The RA50H8994M1 is a 50W RF MOSFET Amplifier Module for 12.5V mobile radios that operate in the 896 to 944 MHz range.
The battery can be connected directly to the drain of the enhancement-mode MOSFET transistors. Without the gate voltage 1 and the gate voltage 2(V_{GG1}=V_{GG2}=0V), only a small leakage current flows into the drain and the nominal output signal (P_{out}=50W) attenuates up to 60 dB. When fixed i.e. 3.6V, is supplied to the gate voltage 1, the output power and the drain current increase as the gate voltage 2 increases. The output power and the drain current increase substantially with the gate voltage 2 around 0V (minimum) under the condition when the gate voltage 1 is kept in 3.6V. The nominal output power becomes available at the state that V_{GG2} is 4V (typical) and 5V (maximum). At this point, V_{GG1} has to be kept in 3.6V.
This module is designed for non-linear FM modulation, but may also be used for linear modulation by setting the drain quiescent current with the gate voltages and controlling the output power with the input power.

Terminal arrangement



① INPUT (P_{in}) & GATE1 SUPPLY TERMINAL(V_{GG1})
② GATE2 BIAS DC SUPPLY TERMINAL (V_{GG2})
③ DRAIN BIAS DC SUPPLY TERMINAL (V_{DD})
④ OUTPUT TERMINAL (P_{out})
⑤ FIN (GND)

PACKAGE CODE: H2M(B)

FEATURES

- Enhancement-Mode MOSFET Transistors (I_{DD}≅0 @ V_{DD}=12.5V, V_{GG}=0V)
- P_{out}>50W, η_T>40% @ V_{DD}=12.5V, V_{GG1}=3.6V, V_{GG2}=5V, P_{in}=50mW
- Broadband Frequency Range: 896-944MHz
- Module Size: 67 x 19.4 x 9.9 mm
- Linear operation is possible by setting the quiescent drain current with the gate voltage and controlling the output power with the input power

RoHS COMPLIANCE

- RA50H8994M1 is a RoHS compliant products.
- This product include the lead in the Glass of electronic parts and the lead in electronic Ceramic parts.
  However, it is applicable to the following exceptions of RoHS Directions.
  1.Lead in the Glass of a cathode-ray tube, electronic parts, and fluorescent tubes.
  2.Lead in electronic Ceramic parts.

ORDERING INFORMATION:

ORDER NUMBER	SUPPLY FORM
RA50H8994M1-501	Antistatic tray, 10 modules/tray

MAXIMUM RATINGS (T$_{case}$=+25°C, Z$_G$=Z$_L$=50Ω, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{DD}	Drain Voltage	V_{GG1}=3.6V±7%, V_{GG2}≦5V	17	V
V_{GG1}	Gate Voltage1	V_{DD}≦12.5V, V_{GG2}≦5V, P_{in}=50mW	4.5	V
V_{GG2}	Gate Voltage2	V_{DD}≦12.5V, V_{GG1}=3.6V±7%, P_{in}=50mW	6	V
I_{DD}	Total Current	-	15	A
P_{in}	Input Power	f=896-944MHz, V_{GG1}=3.6V±7%, V_{GG2}≦5V	100	mW
P_{out}	Output Power		65	W
$T_{case(OP)}$	Operation Case Temperature Range		-30 to +100	°C
T_{stg}	Storage Temperature Range	-	-40 to +110	°C

The above parameters are independently guaranteed.

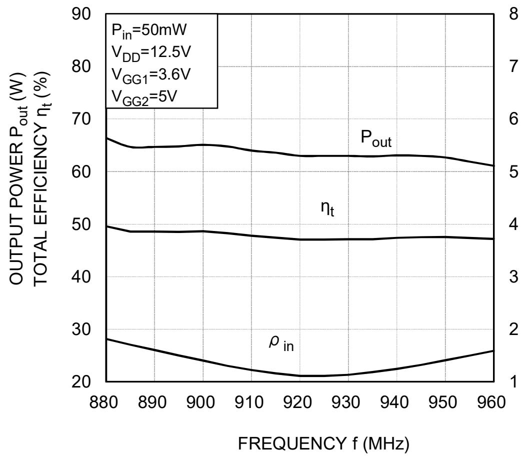
ELECTRICAL CHARACTERISTICS (T$_{case}$=+25°C, Z$_G$=Z$_L$=50Ω, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f	Frequency Range	-	896	-	944	MHz
P_{out1}	Output Power1	V_{DD}=12.5V, V_{GG1}=3.6V, V_{GG2}=5V, P_{in}=50mW	50	-	-	W
η_T	Total Efficiency		40	-	-	%
$2f_0$	2nd Harmonic		-	-	-40	dBc
$3f_0$	3nd Harmonic		-	-	-35	dBc
ρ_{in}	Input VSWR		-	-	3:1	-
I_{DD}	Leakage current	V_{DD}=17V, V_{GG1}= V_{GG2}=0V, Pin=0W	-	-	1	mA
-	Load VSWR Tolerance	V_{DD}=15.2V, V_{GG1}=3.6V, P_{in}=50mW, P_{out}=50W (V_{GG2} : adj.), Load VSWR=20:1(All Phase)	No degradation or destroy			-
-	Stability	V_{DD}=10-15.2V, V_{GG1}=3.6V, P_{in}=1-100mW, P_{out}=1.5-55W (V_{GG2} : control, V_{GG2}≦5V) Load VSWR=3:1(All Phase)	No parasitic oscillation more than -65dBc			-
P_{out2}	Output Power2 *	V_{DD}=12.5V, V_{GG1}=3.6V, V_{GG2}=1V, P_{in}=2dBm	-	-	1.5	W

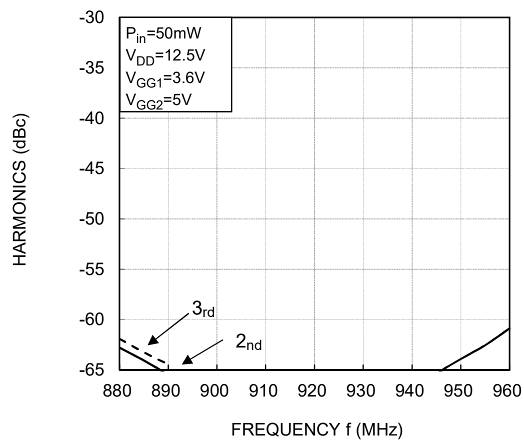
All parameters, conditions, ratings, and limits are subject to change without notice.
* This item is tested at the time first lot and design changes.

TYPICAL PERFORMANCE (T_{case}=+25°C, Z_G=Z_L=50Ω, unless otherwise specified)

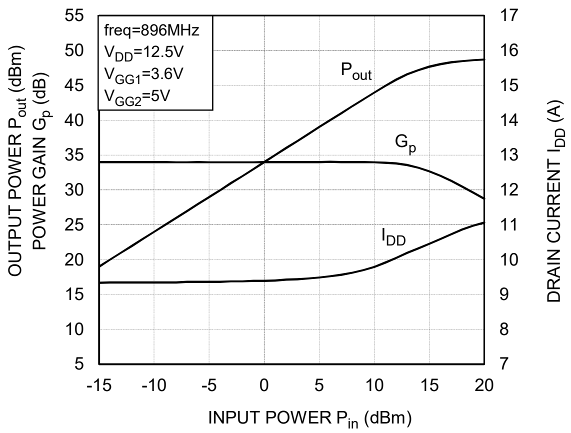
OUTPUT POWER, TOTAL EFFICIENCY, and INPUT VSWR versus FREQUENCY



2nd,3rd HARMONICS versus FREQUENCY



OUTPUT POWER, POWER GAIN and DRAIN CURRENT versus INPUT POWER



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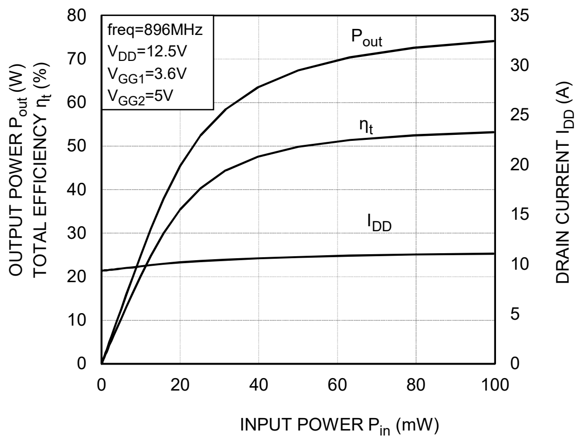

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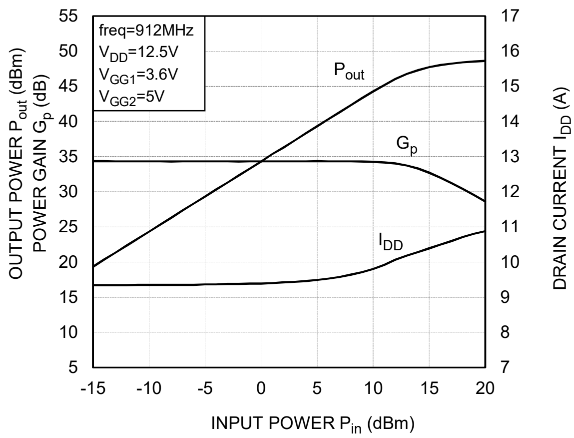
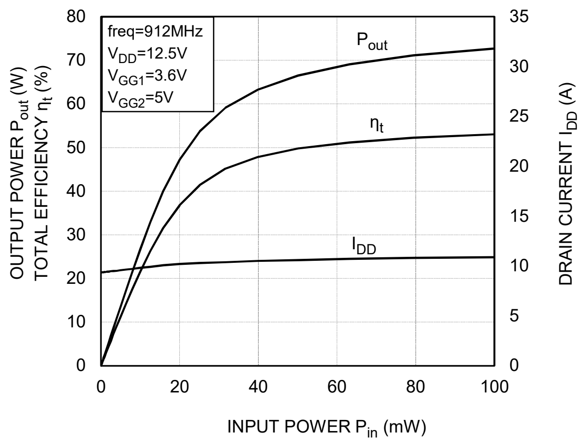
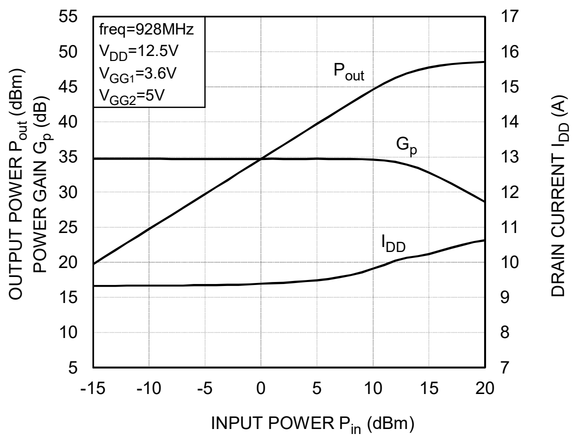


OUTPUT POWER, POWER GAIN and DRAIN CURRENT versus INPUT POWER

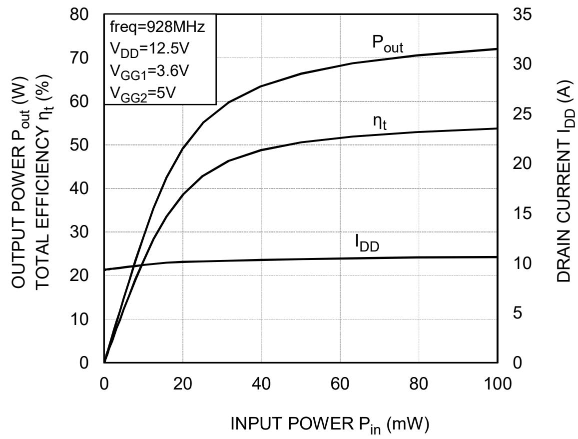


TYPICAL PERFORMANCE
(T_{case}=+25℃, Z_G=Z_L=50Ω, unless otherwise specified)

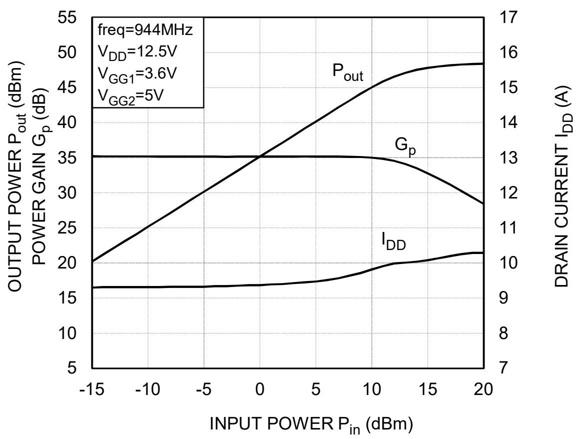
OUTPUT POWER, POWER GAIN and DRAIN CURRENT versus INPUT POWER



OUTPUT POWER, POWER GAIN and DRAIN CURRENT versus INPUT POWER



OUTPUT POWER, POWER GAIN and DRAIN CURRENT versus INPUT POWER



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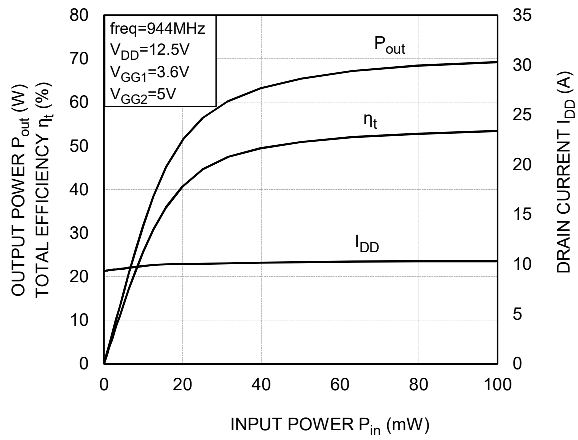
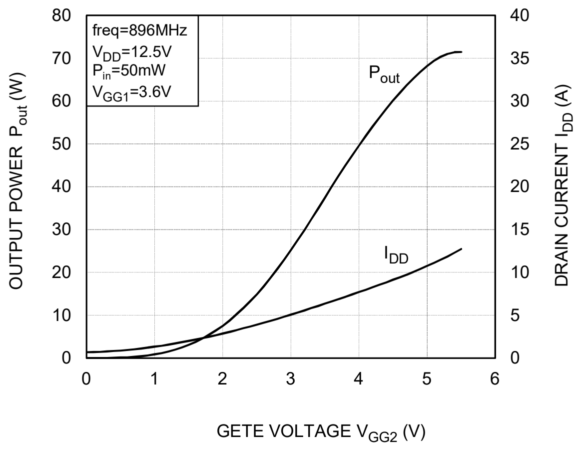
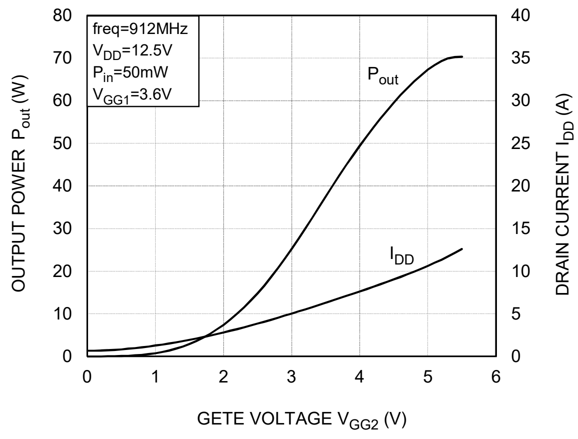


OUTPUT POWER and DRAIN CURRENT versus GATE VOLTAGE 2

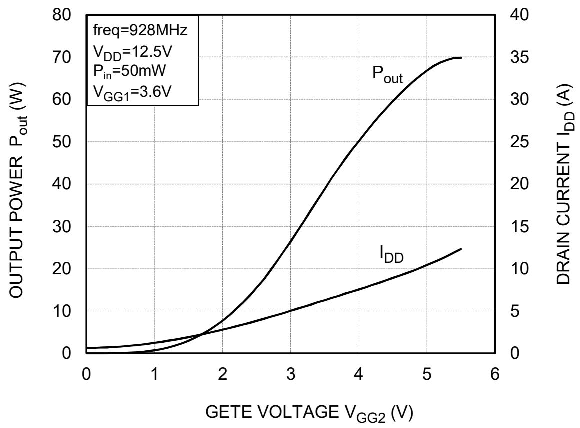


OUTPUT POWER and DRAIN CURRENT versus GATE VOLTAGE 2

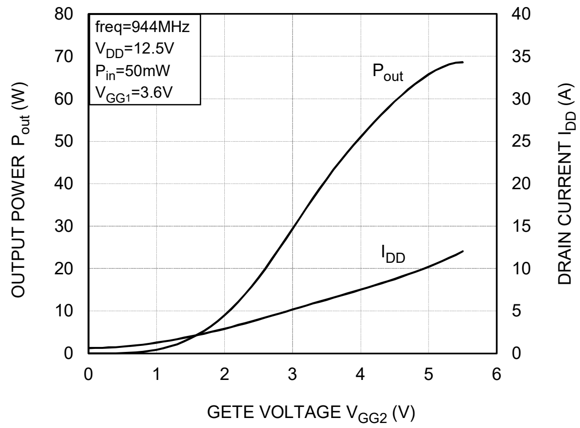


TYPICAL PERFORMANCE (T$_{case}$=+25℃, Z$_G$=Z$_L$=50Ω, unless otherwise specified)

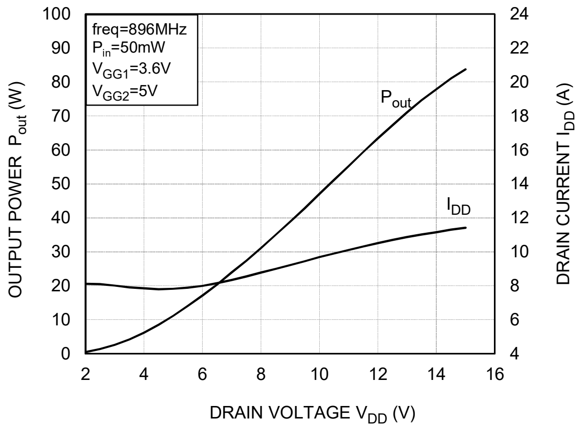
OUTPUT POWER and DRAIN CURRENT versus GATE VOLTAGE 2



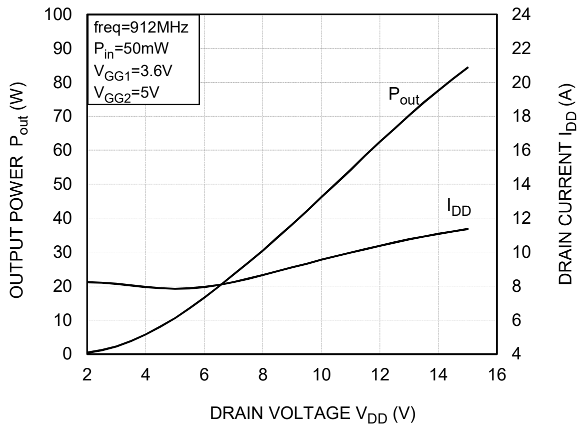
OUTPUT POWER and DRAIN CURRENT versus GATE VOLTAGE 2



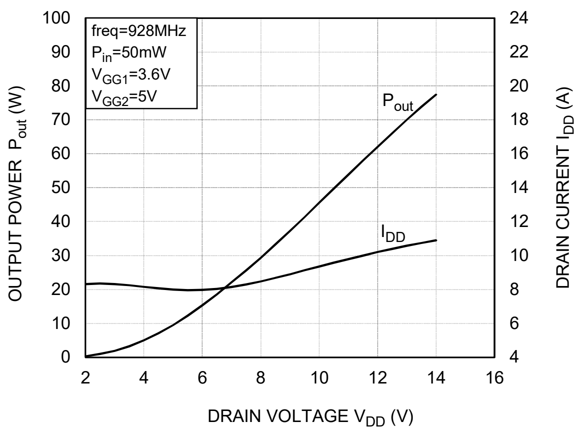
OUTPUT POWER and DRAIN CURRENT versus DRAIN VOLTAGE



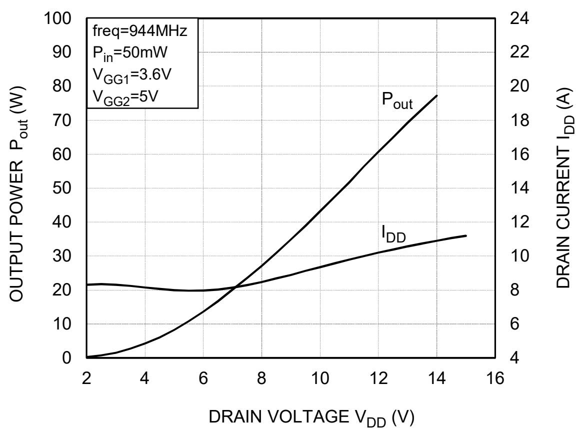
OUTPUT POWER and DRAIN CURRENT versus DRAIN VOLTAGE



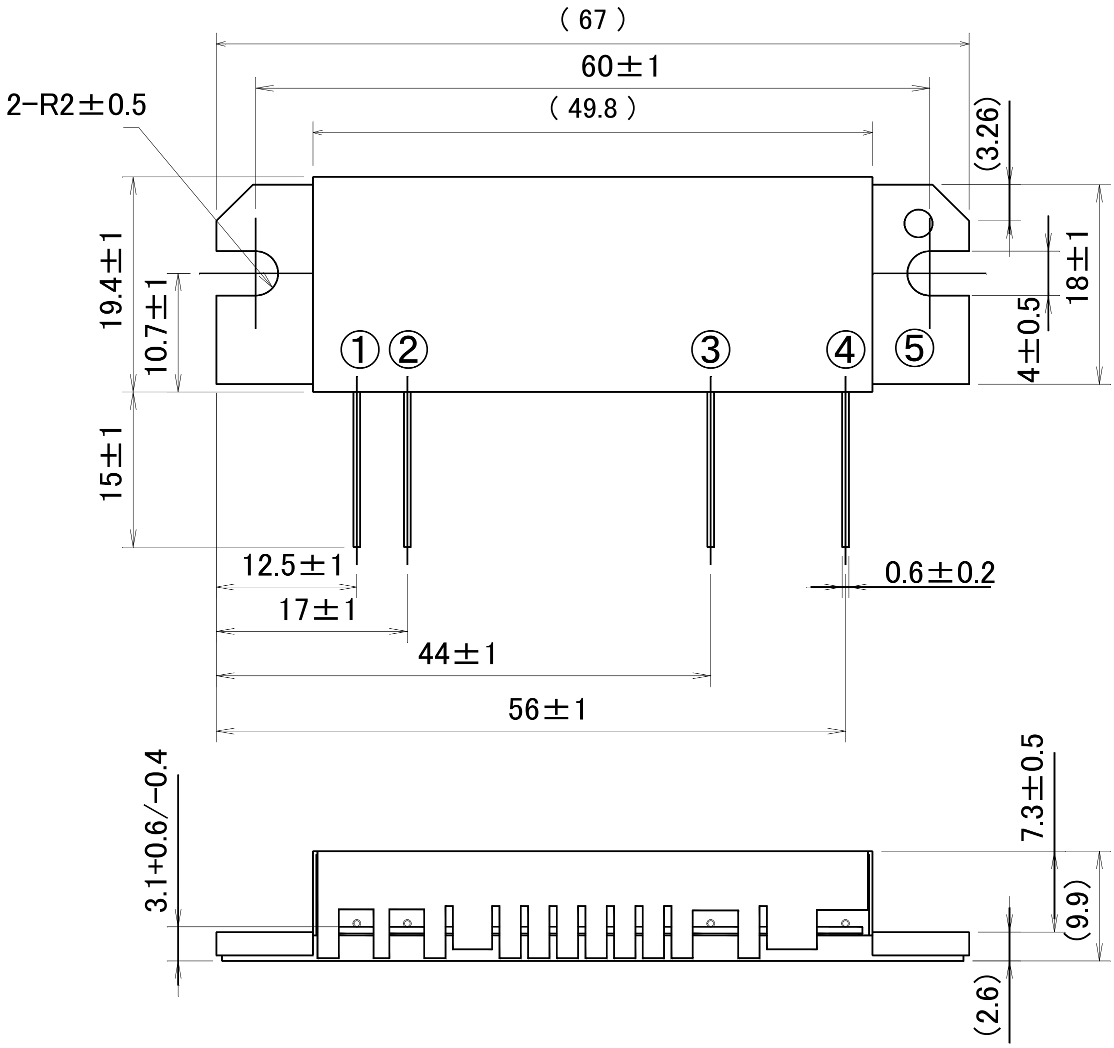
OUTPUT POWER and DRAIN CURRENT versus DRAIN VOLTAGE



OUTPUT POWER and DRAIN CURRENT versus DRAIN VOLTAGE



OUTLINE DRAWING (mm)



① RF Input added Gate Voltage 1(P_{in} & V_{GG1})

② GATE Voltage 2 (V_{GG2})

③ DRAIN Voltage (V_{DD})

④ RF Output (P_{out})

⑤ FIN (GND)

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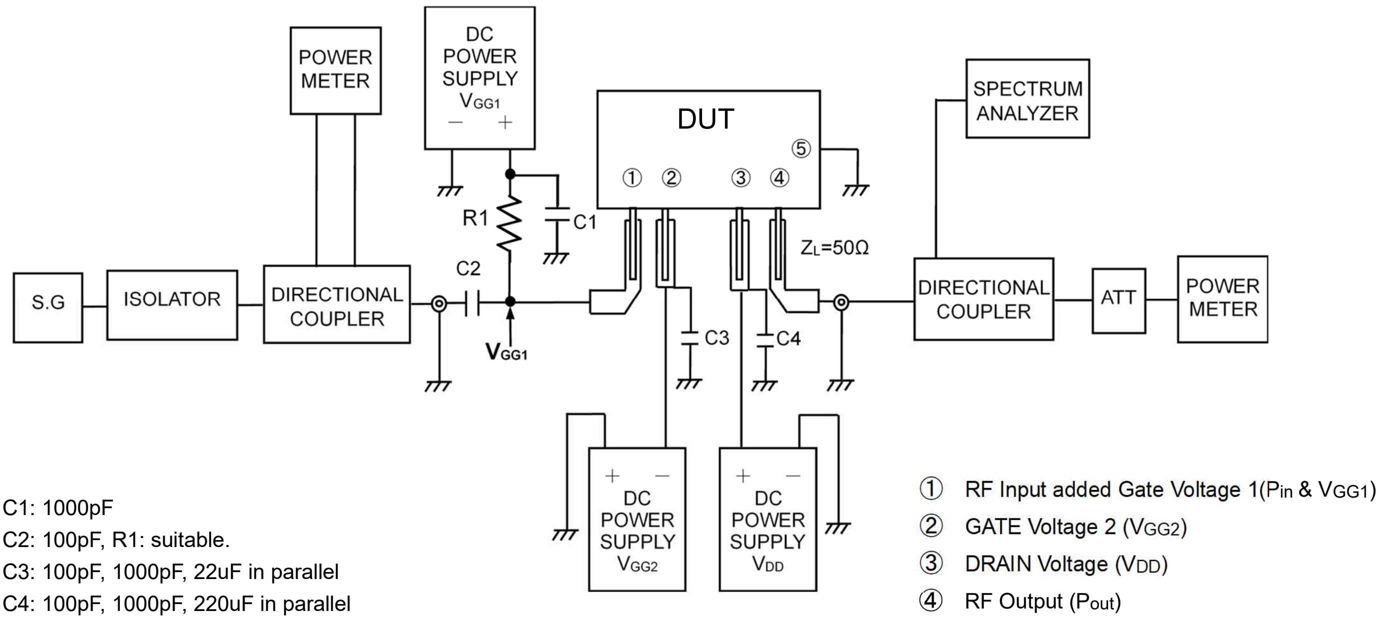
RoHS Compliance, 896-944MHz 50W 12.5V, 2 Stage Amp. For MOBILE Radio

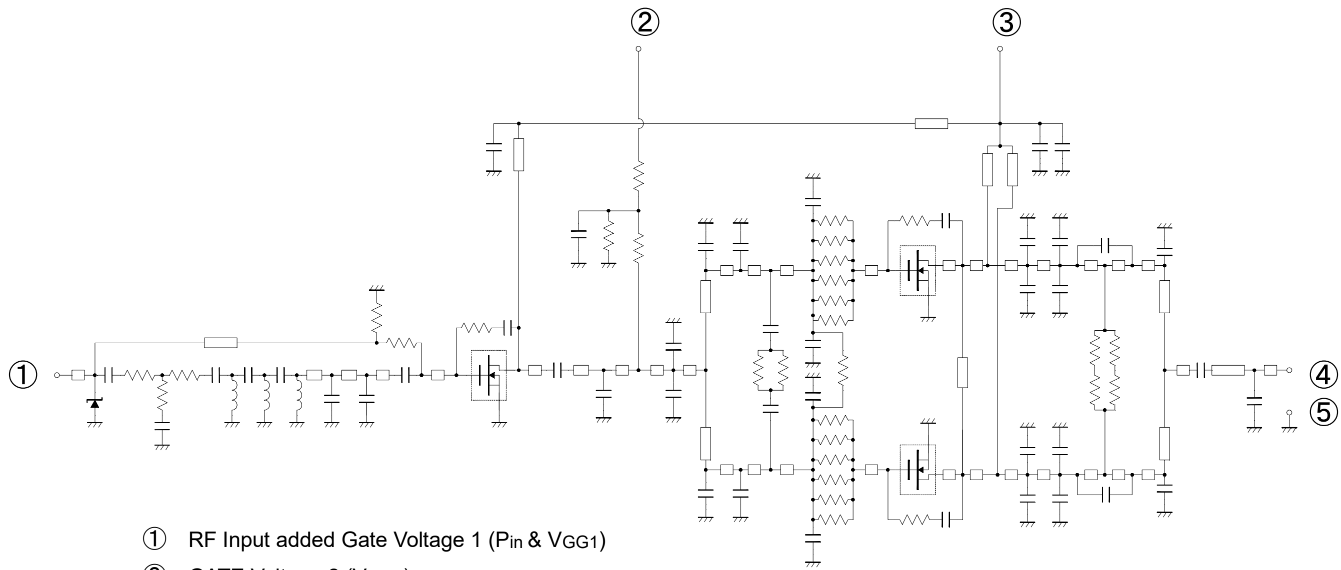
TEST BLOCK DIAGRAM



C1: 1000pF
C2: 100pF, R1: suitable.
C3: 100pF, 1000pF, 22uF in parallel
C4: 100pF, 1000pF, 220uF in parallel
V_{GG1}=3.6V

① RF Input added Gate Voltage 1(P_{in} & V_{GG1})
② GATE Voltage 2 (V_{GG2})
③ DRAIN Voltage (V_{DD})
④ RF Output (P_{out})
⑤ FIN (GND)

EQUIVALENT CIRCUIT



① RF Input added Gate Voltage 1 (P_{in} & V_{GG1})
② GATE Voltage 2 (V_{GG2})
③ DRAIN Voltage (V_{DD})
④ RF Output (P_{out})
⑤ FIN (GND)

NOTE: Resistance between Gate Voltage 1, where RF is input, and ground equals to 15k ohm.
External resistance connected to V_{GG1}; impedance between P_{in}&V_{GG1} and ground needs to make high impedance that doesn't prevent RF characteristic on this module.

< Silicon RF Power Module >

RECOMMENDATIONS and APPLICATION INFORMATION:

Construction:

This module consists of a glass-epoxy substrate soldered onto a copper flange. For mechanical protection, a metal cap is attached (which makes the improvement of RF radiation easy). The MOSFET transistor chips are die bonded onto metal, wire bonded to the substrate, and coated with resin. Lines on the substrate (eventually inductors), chip capacitors, and resistors form the bias and matching circuits. Wire leads soldered onto the glass-epoxy substrate provide the DC and RF connection.

Following conditions must be avoided:

a) Bending forces on the glass-epoxy substrate (for example, by driving screws or from fast thermal changes)
b) Mechanical stress on the wire leads (for example, by first soldering then driving screws or by thermal expansion)
c) Defluxing solvents reacting with the resin coating on the MOSFET chips (for example, Trichloroethylene)
d) ESD, surge, overvoltage in combination with load VSWR, and oscillation

ESD:

This MOSFET module is sensitive to ESD voltages down to 1000V. Appropriate ESD precautions are required.

Mounting:

A thermal compound between module and heat sink is recommended for low thermal contact resistance. The module must first be screwed to the heat sink, then the leads can be soldered to the printed circuit board.
M3 screws are recommended with a tightening torque of 4.0 to 6.0 kgf-cm.

Soldering and Defluxing:

This module is designed for manual soldering.
The leads must be soldered after the module is screwed onto the heat sink.
The temperature of the lead (terminal) soldering should be lower than 350°C and shorter than 3 second.
Ethyl Alcohol is recommend for removing flux. Trichloroethylene solvents must not be used (they may cause bubbles in the coating of the transistor chips which can lift off the bond wires).

Thermal Design of the Heat Sink:

At P_{out}=50W, V_{DD}=12.5V and P_{in}=50mW each stage transistor operating conditions are:

Stage	P_{in} (W)	P_{out} (W)	$R_{th(ch-case)}$ (°C/W)	I_{DD} @ η_T=40% (A)	V_{DD} (V)
1st	0.05	4.0	2.5	0.8	12.5
2nd	4.0	50	0.57	9.2	

The channel temperatures of each stage transistor $T_{ch} = T_{case} + (V_{DD} \times I_{DD} - P_{out} + P_{in}) \times R_{th(ch-case)}$ are:

$T_{ch1} = T_{case}$ + (12.5V x 0.8A – 4.0W + 0.05W) x 2.5°C/W= T_{case} + 15.1 °C

$T_{ch2} = T_{case}$ + (12.5V x 9.2A – 50.0W + 4.0W) x 0.57°C/W= T_{case} + 39.3 °C

For long-term reliability, it is best to keep the module case temperature (T_{case}) below 90°C. For an ambient temperature T_{air}=60°C and P_{out}=50W, the required thermal resistance $R_{th\ (case-air)} = (T_{case} - T_{air}) / ((P_{out} / \eta_T) - P_{out} + P_{in})$ of the heat sink, including the contact resistance, is:

$R_{th(case-air)}$ = (90°C - 60°C) / (50W/40% - 50W + 0.05W) = 0.4 °C/W

When mounting the module with the thermal resistance of 0.4 °C/W, the channel temperature of each stage transistor is:

$T_{ch1} = T_{air}$ + 45.1 °C

$T_{ch2} = T_{air}$ + 69.3°C

The 175°C maximum rating for the channel temperature ensures application under derated conditions.

Keep safety first in your circuit designs!

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